# M1701

16-Channel Form A **M1702** 

4X4 Matrix Switch M1703

**Dual 8-to-1 Relay** 

PUBLICATION NO. 980882

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This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.



If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.



Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.



Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid "live" circuit points.

Before operating this instrument:

- 1. Ensure the proper fuse is in place for the power source to operate.
- 2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

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# Chapter 1 Getting Started

# What's in this Manual?

This manual contains module descriptions, configuration and wiring information, register programming information, and specifications for these M-Modules:

- Racal M1701 16-Channel Form A Switch (P/N 407871)
- Racal M1702 4x4 Matrix Switch (P/N 407872)
- Racal M1703 Dual 8-to-1 Relay Multiplexer (P/N 407873)

In this manual, where the information is identical for all three M-Modules, they will be referred to collectively as the *Switch M-Modules*. Differences between the modules include switching schematics, wiring diagrams, channel numbering, and specifications. These differences are documented individually for each module.

The Switch M-Modules are intended to be installed on an M-Module Carrier. When it is necessary to reference a particular carrier, the C&H Technologies Model VX405C VXIbus M-Module Carrier will be used. Refer to the User Manual for the M-Module Carrier used.

# **Caution** The Switch M-Modules use latching relays that retain their last programmed state whenever power is removed.

If you are programming at the register level, THESE RELAYS DO NOT RESET THEMSELVES AUTOMATICALLY WHEN POWER IS RE-APPLIED. This means that closed relays will remain closed when power is re-applied, and will stay closed until you open them programmatically.

If you are using the D-SCPI driver, the driver WILL open all Switch M-Module relays shortly after power is re-applied to the Command Module.

Caution The Switch M-Modules DO NOT have provision for on-board current limiting components. If it is possible that input current could exceed 2 A DC or 2 A AC-Peak per channel, you must install external current limiting circuitry.

# **Module Descriptions**

| General Product<br>Features                     | <ul> <li>FIFO register structure allows fast system operation.</li> <li>Standard 44-Pin D-Sub connectors provide a common interface to all three Switch M-Modules.</li> <li>Single-width M-Modules provide high-density and maximum flexibility of configuration.</li> <li>Low-cost switching in VXI environment when used in an C&amp;H Technologies Model VX405C.</li> </ul>   |
|---|--|
| Racal M1701<br>16-Channel Form A<br>Switch      | The Racal M1701 is a general purpose relay switch consisting of 16 one-wire switches on a single-width M-Module. This module can be used to connect test points on a device under test to instrumentation or to switch factory automation and fixturing. The switching schematic and user connector diagram are shown in Figure 1-2 on page 1-5.   |
| Racal M1702 4x4<br>Matrix Switch                | The Racal M1702 is a 4x4 matrix consisting of 16 DPST relays configured<br>as 4 rows and 4 columns of two-wire switches. This module can connect<br>multiple instruments to multiple points in your test system. This provides<br>flexible interconnections between test points, instrumentation, factory<br>automation, and test fixtures. The switching schematic and user connector<br>diagram are shown in Figure 1-3 on page 1-6. |
| Racal M1703 Dual<br>8-to-1 Relay<br>Multiplexer | The Racal M1703 provides two separate 8-to-1, two-wire multiplexers.<br>Alternatively, you can move a jumper to connect the common channels of<br>each multiplexer together and create a single 16-to-1, two-wire multiplexer.<br>The switching schematic and user connector diagram are shown in Figure<br>1-4 on page 1-7.   |

# Wiring and Configuration

This section describes how to connect user wiring to each of the three Switch M-Modules. It also describes how to configure the Racal M1703 as a dual 8-to-1 or a single 16-to-1 multiplexer.

**Note** The procedures in this section assume the M-Module(s) have already been installed into an M-Module Carrier. Since installation is dependent on the carrier used, instructions for installing M-Modules into the carrier are not included here. Refer to your M-Module carrier documentation for installation instructions. Each Racal Instruments M-Module is shipped with identifying labels that you should install on the carrier.

Identfying<br/>M-ModulesThe Switch M-Modules have a module ID number printed on the PC-board.<br/>The ID number consists of a model number prefix/PC-board number suffix.<br/>For example, "M1701" is the ID number for the Racal M1701 M-Module.<br/>ID number locations are shown in Figures 1-2, 1-3, and 1-4.

WARNING SHOCK HAZARD. Only service-trained personnel who are aware of the hazards involved should install, remove, or configure the modules. Before installing or removing any module or carrier, disconnect power from the mainframe and user wiring.

Caution MAXIMUM VOLTAGE/CURRENT. The maximum voltage that may be applied to any connector on the Racal M1701, M1702, or M1703 is 200 VDC, 125 VAC rms, or 175 VAC peak. These limits apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and NO relay connection is made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak. The maximum current (non-inductive) that may be appied to the Racal M1701, M1702, or M1703 is:

> Per Switch: 2 ADC, 2 AAC peak Per Module: 8 ADC, 8 AAC peak

Caution STATIC ELECTRICITY. Static electricity is a major cause of component failure. To prevent damage to the electrical components on an M-Module or the carrier, observe anti-static techniques whenever installing, removing, or working on a carrier or M-Module.

## Assembling the Field Wiring Connector

Each Switch M-Module includes a 44-pin connector and hood. You must supply your own cable. The drawing below shows how to connect wiring and assemble the connector and hood.

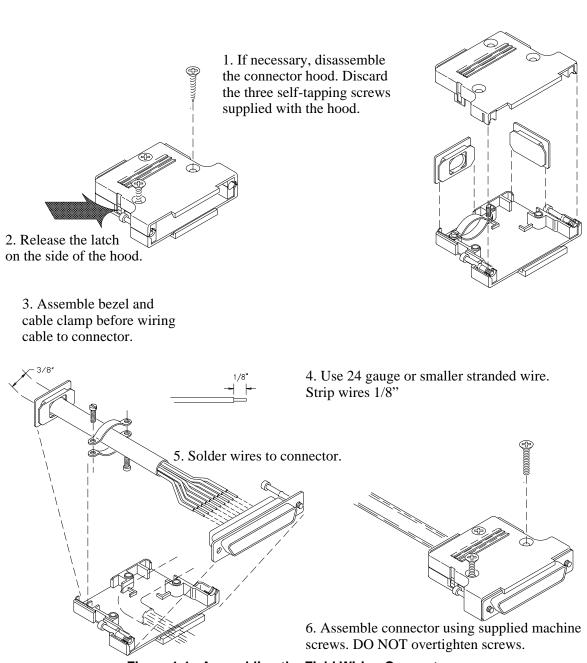
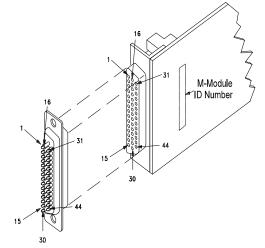


Figure 1-1. Assembling the Field Wiring Connector

## **Racal M1701 Form A Switch Wiring Information**



MAXIMUM VOLTAGE/CURRENT. The maximum voltage that may be applied to any connector on the Racal M1701, M1702, or M1703 is 200 VDC, 125 VAC rms, or 175 VAC peak--these limits apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and there is NOT a relay connection made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

The maximum current (non-inductive) that may be applied to the Racal M1701, M1702, or M1703 is:

Per Switch: 2 ADC, 2 AAC peak Per Module: 8 ADC, 8 AAC peak

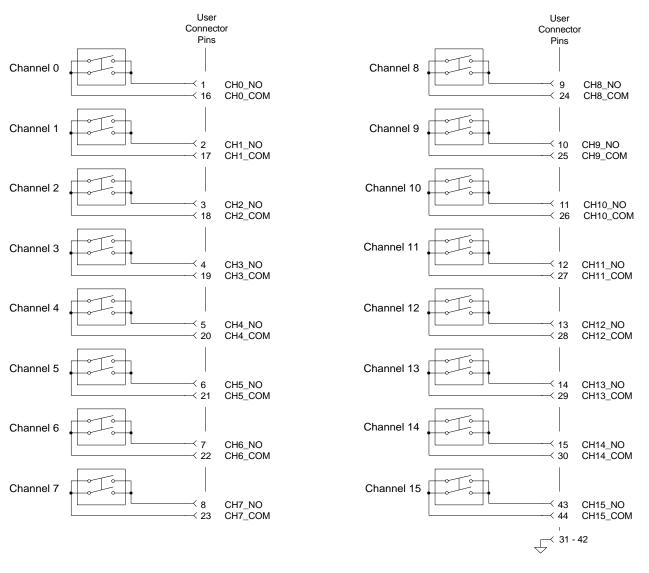
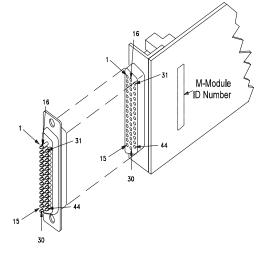


Figure 1-2. Racal M1701 User Connector and Switching Schematic

## **Racal M1702 4x4 Matrix Switch Wiring Information**



MAXIMUM VOLTAGE/CURRENT. The maximum voltage that may be applied to any connector on the Racal M1701, M1702, or M1703 is 200 VDC, 125 VAC rms, or 175 VAC peak--these limits apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and there is NOT a relay connection made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

The maximum current (non-inductive) that may be applied to the Racal M1701, M1702, or M1703 is:

Per Switch: 2 ADC, 2 AAC peak Per Module: 8 ADC, 8 AAC peak

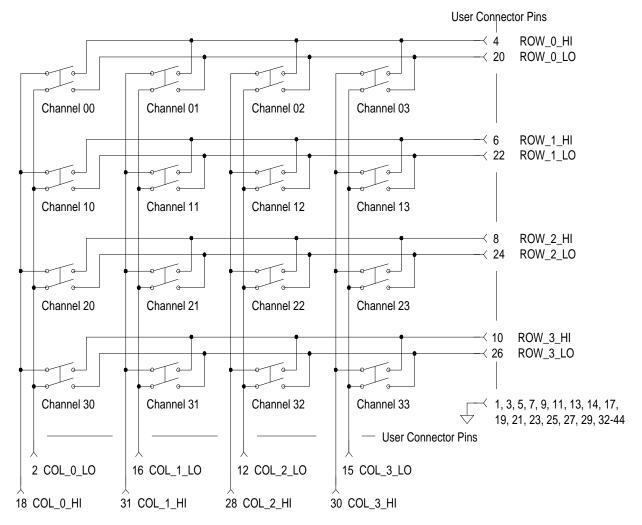
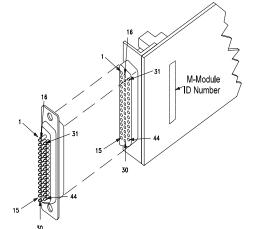


Figure 1-3. Racal M1702 User Connector and Switching Schematic

## Racal M1703 Dual 8-to-1 Relay Multiplexer Wiring Information



MAXIMUM VOLTAGE/CURRENT. The maximum voltage that may be applied to any connector on the Racal M1701, M1702, or M1703 is 200 VDC, 125 VAC rms, or 175 VAC peak--these limits apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and there is NOT a relay connection made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

The maximum current (non-inductive) that may be applied to the Racal M1701, M1702, or M1703 is:

Per Switch: 2 ADC, 2 AAC peak Per Module: 8 ADC, 8 AAC peak

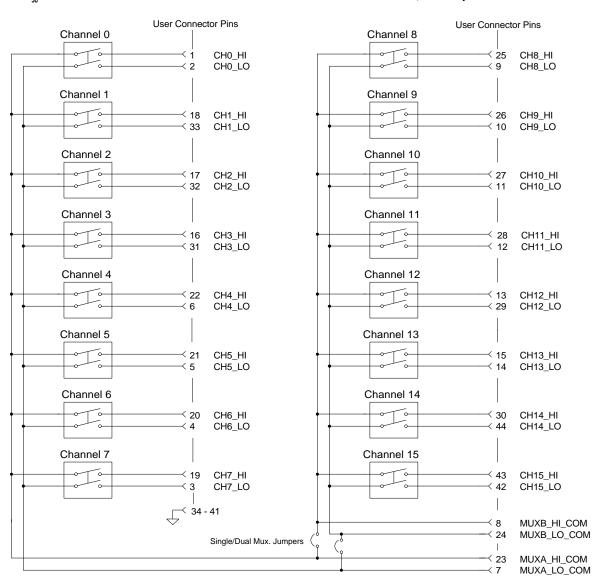


Figure 1-4. Racal M1703 User Connector and Switching Schematic

## Setting Racal M1703 Multiplexer Size

Figure 1-4 shows the two jumper positions for the Racal M1703. When in position A (jumper **not** connecting one row of pins), the module is configured as a dual 8-to-1 multiplexer. When in position B (jumper connecting all pins), the module is configured as a single 16-to-1 multiplexer. The Racal M1703 leaves the factory with the jumper placed in position A (dual 8-to-1 multiplexer). If you need to change this jumper postion, it must be done **before** installing the M-Module onto the carrier.

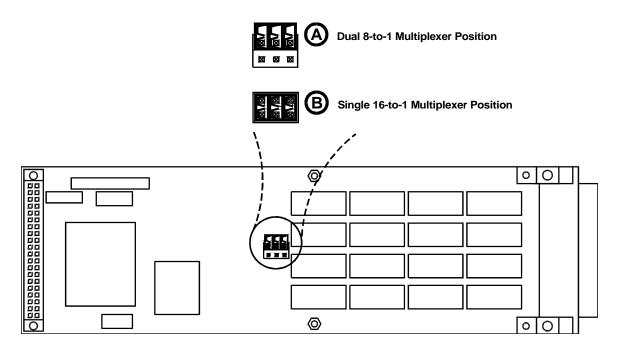


Figure 1-5. Racal M1703 Jumper Positions

# Introduction

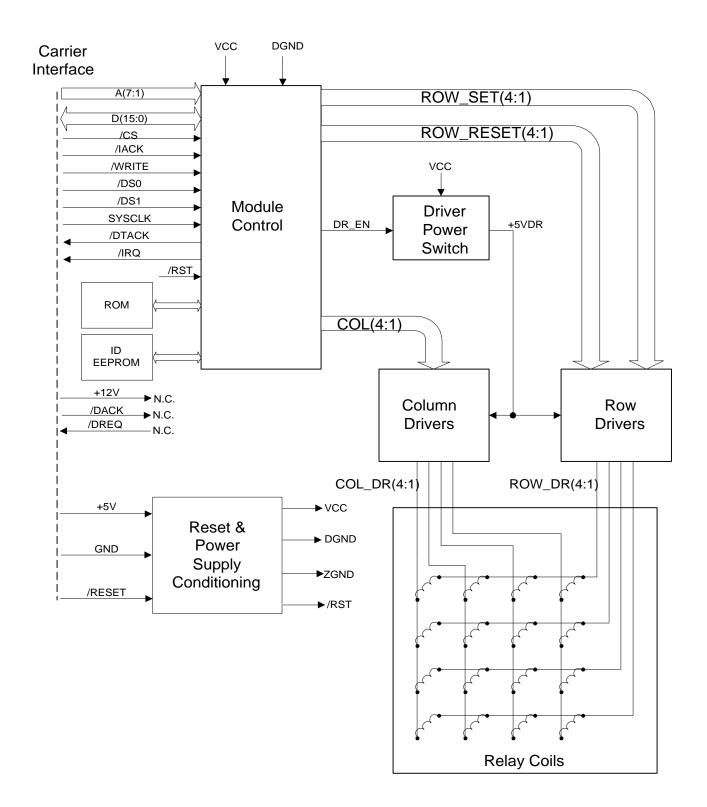
This chapter describes how to program the Switch M-Modules at the register level in an C&H Technologies Model VX405C Carrier installed in a VXIbus mainframe. Register programming is recommended only if you are unable to use the module's higher-level VXI*plug&play* driver. For information on using the VXI*plug&play* driver, refer to the on-line help.

# **Block Diagram Description**

In order to register program a Switch M-Module, it is important to understand its operation at the block diagram level. The block diagram is identical for all three Switch M-Modules. All three have identical register maps and identical row and column matrix drive schemes. The only conceptual differences are the three different switch topologies (form A, multiplexer, matrix). Figure 2-1 on page 2-3 shows the Switch M-Modules block diagram and the following paragraphs describe each block. **Module Control** This block contains the logic for the module including all registers, FIFO and FIFO control and interrupt control. **FIFO Structure** The FIFO (First-In-First-Out) structure allows multiple writes to the module to be stacked-up. This helps reduce interrupt overhead by allowing an interrupt only after the completion of the last relay operation in a sequence of up to eight operations. Eight was chosen because it allows at least one open and one close to each of the four relay rows--allowing a complete change of all relay states. If the M-Module is enabled to interrupt, it asserts the INTn line on the M-Module interface to the Carrier when the last commanded relay operation in the FIFO has completed. For example, if relays in only one row were instructed to move, the module asserts an interrupt after that one row has been driven. If four rows were instructed to move (four writes to the FIFO--see Note below), then the module asserts an interrupt only after the

completion of the fourth operation.

| Note                            | The module asserts an interrupt after the relay drive time is complete (relay drive timer) and no other operations have been stored in FIFO. The above example assumes the four writes are stored in FIFO one after the other with very little time between the writes. If, in the above example, the amount of time between writes is greater than the relay drive time (8 msec), the module would actually interrupt four timesone interrupt after driving each relay.                              |
|---------------------------------|---|
| ID EEPROM                       | The EEPROM holds sixty-four 16-bit words of M-Module ID data and VXI M-Module data. Refer to Table 2-24, "ID EEPROM Contents," on page 2-20 for EEPROM contents.  |
| Row and Column<br>Drivers       | All of the Switch M-Modules use a matrix drive scheme (rows and columns) in which a maximum of four of the relays (one row) can be operated at any one time. An on-board timer (part of Module Control block) ensures the relay coils have been driven long enough for the contacts to move and settle.   |
|                                 | The Row Driver block translates the <b>ROW_SET(4:1)</b> and<br><b>ROW_RESET(4:1)</b> command lines from the Module Control block into<br>bipolar and tri-state capable buffered drive signals. The <b>ROW_DR(4:1)</b><br>signals provide either current source from the + <b>5VDR</b> supply (relay set),<br>current sink to ground (relay reset), or tri-stated output (both current-source<br>and current-sink off). Each output is tri-stated whenever that particular row<br>is not being driven. |
|                                 | The Column Driver block translates the <b>COL(4:1)</b> command lines from<br>Module Control into the bipolar buffered drive signals, <b>COL_DR(4:1)</b> . The<br><b>COL_DR(4:1)</b> signals provide either current source from the + <b>5VDR</b><br>supply (relay reset) or current sink to ground (relay set).   |
| Driver Power<br>Switch          | This block removes all power from the Row and Column Driver circuitry<br>except when needed to move relays. This FET switch is open at power-up to<br>prevent any relay contact movement until register writes cause drive-power<br>to be applied.  |
| Relay Coils                     | This block contains the 16 relay coils arranged as a 4x4 matrix. To close a relay, a ROW_DR line sources current while a COL_DR line sinks current to ground. To open a relay, a COL_DR line sources current while a ROW_DR line sinks current to ground. Refer to Figures 1-1, 1-2, and 1-3 for relay switching schematics.  |
| Reset and Power<br>Conditioning | This block filters +5V power to produce VCC power (+5V) for logic and isolates the various grounds used by the module. This block also processes the /RESET signal from the Carrier Interface and monitors power to produce the /RST reset signal for the module.   |





# **Register Addressing in the VXIbus Environment**

| Logical Address           | Each module in a VXIbus (VXI) system, whether VXI or M-Module, must<br>have a unique logical address. The C&H Technologies Model VX405C<br>Carrier provides a logical address for each installed M-Module. Refer to the<br>Model VX405C Installation and Wiring Manual for details (if you are using<br>a different carrier, refer to that carrier's documentation for register-based<br>addressing information).  |
|---------------------------|--|
| A16/A24 Memory<br>Mapping | The VXI Specification allows for only 64 bytes of address space in A16 memory. However, the M-Module Specification defines 256 bytes of address space. To resolve this conflict, the Model VX405C Carrier provides two memory segments for each installed M-Module. The first is in the VXI A16 memory space and contains the standard VXI registers. The second memory segment is in the VXI A24 memory space and contains all other M-Module registers (these registers are described starting on page 2-13). Figure 2-2 shows the A16/A24 mapping for a typical M-Module. |
| Note                      | The M-Module's ID word (from the ID EEPROM) is mapped into the VXI Manufacturer ID Register at address $00_h$ and the M-Module's VXI Device Type word is mapped into the VXI Device Type Register at address $02_h$  |

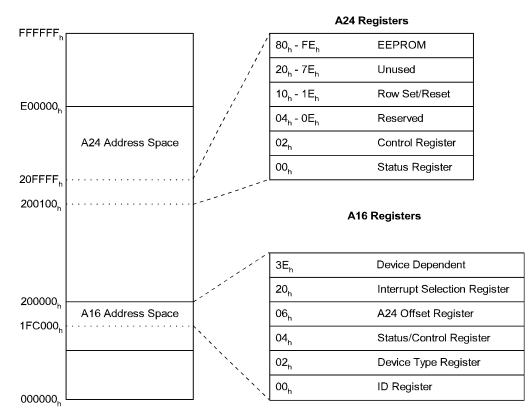


Figure 2-2. A16/A24 Register Mapping

# Determining a Module's A16 Base Address

To access a register in A16 memory, you must specify a hexadecimal or decimal register address. This address consists of a base address plus a register offset. The A16 base address depends on whether or not you are using an GPIB Slot 0 Command Module.

When <u>using</u> a GPIB Slot 0 Command Module, the base address is computed as:

 $1FC000_{h} + (LADDR_{h} \cdot 40_{h})$ or (decimal) 2,080,768 + (LADDR \cdot 64)

Where:

 $1FC000_h$  (2,080,768) is the A16 starting address LADDR is the module's logical address  $40_h$  (64) is the number of address bytes allocated per module

For example, if the M-Module has a logical address of  $78_h$  (120) the A16 base address becomes:

 $1FC000_{h} + (78_{h} \cdot 40_{h}) = 1FC000_{h} + 1E00_{h} = 1FDE00_{h}$ or (decimal)  $2,080,768 + (120 \cdot 64) = 2,080,768 + 7680 = 2,088,448$ 

When a GPIB Slot 0 Command Module is <u>not</u> part of your system, the base address is computed as:

 $\begin{array}{c} \text{C000}_{\text{h}} + (\text{LADDR}_{\text{h}} \cdot 40_{\text{h}}) \\ or (\text{decimal}) \\ 49,152 + (\text{LADDR} \cdot 64) \end{array}$ 

Where:

 $\begin{array}{l} C000_h~(49,152)~is~the~A16~starting~address\\ LADDR~is~the~module's~logical~address\\ 40_h~(64)~is~the~number~of~address~bytes~allocated~per~module\\ \end{array}$ 

For example, if the M-Module has a logical address of  $78_{\rm h}$  (120) the A16 base address becomes:

 $\begin{aligned} \text{C000}_{\text{h}} + (78_{\text{h}} \cdot 40_{\text{h}}) &= \text{C000}_{\text{h}} + 1\text{E00}_{\text{h}} = \text{DE00}_{\text{h}} \\ or \quad (\text{decimal}) \\ 49,152 + (120 \cdot 64) &= 49,152 + 7680 = 56,832 \end{aligned}$ 

| Addressing<br>A16 Registers | As shown in Figure 2-2 on page 2-5, VXI registers for an M-Module are mapped into A16 address space. To access one of these registers, add the A16 base address to the register offset. For example, an M-Module's VXI Status/Control Register has an offset of $04_h$ . To access this register (assuming the system <u>does not</u> have a GPIB Slot 0), use the register address: |
|-----------------------------|--|
|                             | $1FDE00_{h} + 04_{h} = 1FDE04_{h}$<br>or (decimal)<br>2,088,488 + 4 = 2,088,452  |
| Addressing<br>A24 Registers | As shown in Figure 2-2 on page 2-5, most of the registers for an M-Module are mapped into A24 address space. To access one of these registers:   |
|                             | 1. Obtain the A24 base address by reading the VXI Offset Register $(06_h)$ in A16 memory.  |
|                             | 2. Add the A24 base address to the register offset (see Table 2-7. on page 13).  |
|                             | For example, if the A24 base address is $200100_h$ , to access a Switch M-Module's Row 0 Set Register (10 <sub>h</sub> ):  |
|                             | $200100_{\rm h} + 10_{\rm h} = 200110_{\rm h}$   |

or (decimal) 2,097,408 + 16 = 2,097,424

# **Program Example**

The following C language program can be used with any of the Switch M-Modules and demonstrates how to program at the register level. The program resets (opens) all relays and then closes channels 00 and 02. This program was written and tested in Microsoft Visual C++ but should compile with any standard ANSI C compiler.

To run this program you must have the HP SICL Library, the NI VISA Library, a GPIB interface module installed in your PC, and a GPIB Slot 0 Command Module.

#include <visa.h>
#include <stdio.h>
#include <stdlib.h>

ViSession defaultRM,m\_mod; void err\_handler();

void main(void)

{

/\*ID & device type registers\*/ unsigned short id\_reg, dt\_reg;

/\* create and open a device session \*/ ViStatus err; viOpenDefaultRM (&defaultRM); /\* Command Module is GPIB-VXI0, M-Module logical address is 24 \*/ err = viOpen (defaultRM,"GPIB-VXI0::24",VI\_NULL,VI\_NULL,&m\_mod); if(err < VI\_SUCCESS) { printf("Unable to open session "); return;

}

/\* read and print the M-Module's ID and Device Type Registers \*/ err = viln16(m\_mod,VI\_A16\_SPACE,0x00,&id\_reg); if (err < VI\_SUCCESS) err\_handler(m\_mod,err);

err = viln16(m\_mod,VI\_A16\_SPACE,0x02,&dt\_reg); if (err < VI\_SUCCESS) err\_handler(m\_mod,err);</pre>

printf("ID register = 0x%4X\n", id\_reg); printf("Device Type register = 0x%4X\n", dt\_reg);

/\*Enable driver power to relays\*/ err = viOut16(m\_mod,VI\_A24\_SPACE,0x02,0x08); if (err < VI\_SUCCESS) err\_handler(m\_mod,err);

/\*Reset all relays by writing zeros to row reset registers\*/ err = viOut16(m\_mod,VI\_A24\_SPACE,0x12,0x0); err = viOut16(m\_mod,VI\_A24\_SPACE,0x16,0x0); err = viOut16(m\_mod,VI\_A24\_SPACE,0x1A,0x0); err = viOut16(m\_mod,VI\_A24\_SPACE,0x1E,0x0);

```
if (err < VI_SUCCESS) err_handler(m_mod,err);
   /*Close Channels 00 and 02*/
   err = viOut16(m_mod,VI_A24_SPACE,0x10,0x05);
   if (err < VI_SUCCESS) err_handler(m_mod,err);
   /*Close Session */
   viClose (m mod);
   viClose (defaultRM);
}
void err handler ()
/* Error Handling Routine */
   {
   ViStatus err;
   char err_msg[1024] = \{0\};
   viStatusDesc(m_mod,err,err_msg);
   if (strcmp ("VI_SUCCESS: No error",err_msg) != 0)
   printf("ERROR = %s\n",err_msg);
   return;
   }
/* End of Error Handling Routine */
```

# Switch M-Module A16 Register Descriptions

When installed in an Model VX405C Carrier, the Switch M-Modules have the following A16 register definitions.

| Word Address<br>(Offset from A16 Base) | Register Name                       | Register Type |
|--|-------------------------------------|---------------|
| 20 <sub>h</sub>                        | M-Module Interrupt Control Register | Read/Write    |
| 06 <sub>h</sub>                        | A24 Offset Register                 | Read Only     |
| 04 <sub>h</sub>                        | VXI Status/Control Register         | Read/Write    |
| 02 <sub>h</sub>                        | VXI Device Type Register            | Read Only     |
| 00 <sub>h</sub>                        | VXI ID Register                     | Read Only     |

### VXI ID Register

This register contains the M-Module's Device Class, Address Space, and Manufacturer ID.

#### Table 2-1. VXI ID Register (Read Only) Base + $00_h$

| Bit Number | 15 - 14      | 13 - 12       | 11 - 00         |
|------------|--------------|---------------|-----------------|
| Bit Name   | Device Class | Address Space | Manufacturer ID |

# **Bit Definitions** Device Class -- 00 = memory module, 01 = extended memory, 10 = message-based device, 11 = register based device. Switch M-Modules are register-based devices (11).

Address Space -- indicates the M-Modules addressing mode. 00 = A16/A24, 01 = A16/A32, 10 = reserved, 11 = A16 only. Switch M-Modules are A16/A24 (00).

**Manufacturer ID** = 4091 for Racal Instruments.

# VXI Device Type<br/>RegisterThis register contains the M-Module's required memory and model code..RegisterTable 2-2. VXI Device Type Register (Read Only) Base + 02h

| Bit Number | 15 - 12         | 11 - 00             |
|------------|-----------------|---------------------|
| Bit Name   | Required Memory | M-Module Model Code |

**Bit Definitions** 

**ns Required Memory** -- indicates the amount of memory required by the M-Module.

| Bits 15 - 12 | Memory Required | Bits 15 - 12 | Memory Required |
|--------------|-----------------|--------------|-----------------|
| 1111         | 256 Bytes       | 0111         | 64 kBytes       |
| 1110         | 512 Bytes       | 0110         | 128 kBytes      |
| 1101         | 1 kBytes        | 0101         | 256 kBytes      |
| 1100         | 2 kBytes        | 0100         | 512 kBytes      |
| 1011         | 4 kBytes        | 0011         | 1 MBytes        |
| 1010         | 8 kBytes        | 0010         | 2 MBytes        |
| 1001         | 16 kBytes       | 0001         | 4 MBytes        |
| 1000         | 32 kBytes       | 0000         | 8 MBytes        |

**M-Module Model Code** -- M1701 = F25B<sub>h</sub>, M1702 = F25C<sub>h</sub>, M1703 = F25D<sub>h</sub>.

### VXI Status/Control Register

This read/write register controls the module and indicates its status.

#### **Control Register**

When writing to this register, it is a Control Register with the following bit definitions:.

#### Table 2-3. VXI Control Register (Write) Base $04_h$

| Bit Number | 15         | 14 - 02  | 01              | 00    |
|------------|------------|----------|-----------------|-------|
| Bit Name   | A24 Enable | Reserved | Sysfail Inhibit | Reset |

**A24 Enable** -- Writing a logic "1" to this bit enables access to the module's A24 registers.

**Sysfail Inhibit** -- Writing a logic "1" to this bit disables the M-Module from driving the SYSFAIL\* line.

**Reset** -- Writing a logic "1" to this bit resets the Switch M-Module's registers. This does not open any closed relays (see "Program Example" on page 8 for details on how to open all relays).

# **Status Register** When reading from this register, it is a Status Register with the following bit definitions:.

| Table 2-4. VXI St | atus Register | (Read) B | ase $04_{h}$ |
|-------------------|---------------|----------|--------------|
|-------------------|---------------|----------|--------------|

| Bit Number | 15         | 14     | 13 - 04                   | 03    | 02     | 01 - 00          |
|------------|------------|--------|---------------------------|-------|--------|------------------|
| Bit Name   | A24 Active | MODID* | M-Module Device Dependent | Ready | Passed | Device Dependent |

**A24 Active** -- Reading a logic "1" from this bit means the M-Module's registers in A24 memory can be accessed (default = 1).

**MODID\*** -- Reading a logic "1" from this bit means the M-Module is not selected via the P2 MODID line. A logic "0" indicates the M-Module is selected.

**Ready** -- Reading a logic "1" from this bit means the M-Module is ready to accept commands--a logic "0" means the M-Module is busy and is not ready to accept commands.

**Passed** -- Reading a logic "1" from this bit means the M-Module passed its self-test--reading a logic "0" means it failed.

# **A24 Offset Register** This register contains the value of the base address necessary to access the M-Module's A24 address space.

Table 2-5. A24 Offset Register (Read Only) Base + 06h

| Bit Number | 15 - 00          |
|------------|------------------|
| Bit Name   | A24 Base Address |

### Interrupt Selection Register

This register specifies which interrupt line the M-Module will use. Most Slot 0 Modules service interrupt line 1 by default, so normally you do not need to change the interrupt line.

Table 2-6. Interrupt Selection Register (Read/Write) Base 20h

| Bit Number | 15 - 04  | 03             | 02 - 00            |
|------------|----------|----------------|--------------------|
| Bit Name   | Reserved | Interrupt Type | VXI Interrupt Line |

**Bit Definitions** Interrupt Type -- This bit determines which type of interrupt the M-Module supports. A logic "0" indicates the M-Module supports interrupt types A and B. A logic "1" indicates interrupt type C (type C is the default and also the type supported by the Switch M-Modules).

**VXI Interrupt Line** -- These bits determine which interrupt line is used by the M-Module.

| Bits 2, 1, 0 | Interrupt Line            |
|--------------|---------------------------|
| 000          | None (interrupt disabled) |
| 001          | IRQ1 (default)            |
| 010          | IRQ2                      |
| 011          | IRQ3                      |
| 100          | IRQ4                      |
| 101          | IRQ5                      |
| 110          | IRQ6                      |
| 111          | IRQ7                      |

# Switch M-Module A24 Register Descriptions

Table 2-7 shows the A24 register definitions shared by all three Switch M-Modules. The bits contained in each register are defined on the following pages. Notice that only the registers that actually control the relays can be stored in the FIFO structure (FIFO-able in Table 2-7).

| Word Address<br>(Offset from A24<br>Base) | Register Name        | Register<br>Type | FIFO-able<br>Register (Y/N) |
|---|----------------------|------------------|-----------------------------|
| 00 <sub>h</sub>                           | Status Register      | Read Only        | Ν                           |
| 02 <sub>h</sub>                           | Control Register     | Read/Write       | Ν                           |
| 04 <sub>h</sub>                           | Reserved             | NA               | Ν                           |
| 06 <sub>h</sub>                           | Reserved             | NA               | Ν                           |
| 08 <sub>h</sub>                           | Reserved             | NA               | Ν                           |
| 0A <sub>h</sub>                           | Reserved             | NA               | Ν                           |
| 0C <sub>h</sub>                           | Reserved             | NA               | Ν                           |
| 0E <sub>h</sub>                           | Reserved             | NA               | Ν                           |
| 10 <sub>h</sub>                           | Row 0 Set Register   | Read/Write       | Y                           |
| 12 <sub>h</sub>                           | Row 0 Reset Register | Read/Write       | Y                           |
| 14 <sub>h</sub>                           | Row 1 Set Register   | Read/Write       | Y                           |
| 16 <sub>h</sub>                           | Row 1 Reset Register | Read/Write       | Y                           |
| 18 <sub>h</sub>                           | Row 2 Set Register   | Read/Write       | Y                           |
| 1A <sub>h</sub>                           | Row 2 Reset Register | Read/Write       | Y                           |
| 1C <sub>h</sub>                           | Row 3 Set Register   | Read/Write       | Y                           |
| 1E <sub>h</sub>                           | Row 3 Reset Register | Read/Write       | Y                           |
| 20 <sub>h</sub> - 7E <sub>h</sub>         | Unused               | NA               | Ν                           |
| $80_h - FE_h$                             | ID EEPROM            | Read/Write       | Ν                           |

Table 2-7. A24 Switch Module Registers

# Status Register

This register monitors the module's Interrupt Status, FIFO Status (full or empty), Multiplexer Size (Racal M1703 only), and Init Status.

| Bit Number | 15 - 05 | 04             | 03                  | 02                   | 01                  | 00                  |
|------------|---------|----------------|---------------------|----------------------|---------------------|---------------------|
| Bit Name   | Unused  | Init<br>Status | Multiplexer<br>Size | FIFO Empty<br>Status | FIFO Full<br>Status | Interrupt<br>Status |

#### Table 2-8. Status Register (Read Only) Base + 00<sub>h</sub>

**Reset Condition** -- Bits 15 - 08 = logic "1", Bits 07 - 05 = logic "0"; Bits 04, 01, 00 = logic "0"; Bit 03--see text.

**Bit Definitions** Interrupt Status -- When this bit reads logic "1" the module's interrupt line will be asserted (if interrupts are enabled) on the interface to the carrier. When this bit reads logic "0" the module's interrupt line will not be asserted (if interrupts are enabled).

**FIFO Full Status** -- When this bit reads logic "1" the module's FIFO is currently full. When full, any additional writes to any of the FIFO-able registers (**Row n Set** or **Row n Reset**) are not placed into FIFO and are lost. Such writes are not stored in the **Row n Set/Reset** readback register to indicate they were not accepted.

**FIFO Empty Status** -- When this bit reads logic "1" the module's FIFO is currently empty. When empty, up to eight writes to any of the FIFO-able registers (**Row n Set** or **Row n Reset**) will be stored into FIFO and will be immediately acted upon (until the FIFO is full). Such writes are stored in the **Row n Set/Reset** readback register to indicate they were accepted. When this bit reads logic "0" there are still pending relay operations stacked-up in the FIFO. When combined with the **FIFO Full Status** bit, you can determine whether the FIFO is partially full, totally full or empty. The **FIFO Empty Status** bit can be considered the *Not Busy* indicator for the module.

**Multiplexer Size** (Racal M1703 only) -- When this bit reads logic "0" the Racal M1703 is configured as a single 16-to-1 multiplexer. When this bit reads logic "1" Racal M1703 is configured as a dual 8-to-1 multiplexer. Racal M1703 multiplexer size is controlled by a jumper, refer to Chapter 1 for details.

This bit always reads logic "1" for the Racal M1701 and Racal M1702.

**Init Status** -- When this bit reads logic "0" the module has not been initialized after a power-up or a hard reset (assertion of /RESET from carrier). You can initialize the module by 1) enabling driver power, and 2) writing all four column bits to zero in each **Row n Reset** register. This opens all relays and correlates **Row n Set/Reset** readback to the actual relay positions.

When the Init Status bit reads logic "1" the module has been initialized at least once since the last power-up or /RESET.

# **Control Register**

This register controls module reset (soft reset), interrupt enabling, self-test mode selection, relay driver power enabling, and timer mode selection.

| Bit Number | 15 - 06 | 05                    | 04                    | 03                        | 02                      | 01                  | 00    |
|------------|---------|-----------------------|-----------------------|---------------------------|-------------------------|---------------------|-------|
| Bit Name   | Unused  | Timer<br>Mode<br>Bit2 | Timer<br>Mode<br>Bit1 | Driver<br>Power<br>Enable | Self-<br>Test<br>Enable | Interrupt<br>Enable | Reset |

Table 2-9. Control Register (Read/Write) Base + 02<sub>h</sub>

**Reset condition** -- Bits 15 - 06 = logic "1", Bits 05 - 00 = logic "0"

**Bit Definitions** Reset -- Writing a logic "1" to this bit causes a soft reset of the module while the bit is high. Subsequently writing a logic "0" to this bit releases the module from the reset condition.

**Interrupt Enable** -- Writing a logic "1" to this bit enables the module to interrupt on the M-Module interface to the carrier. Writing a logic "0" to this bit disables the module from asserting interrupts.

**Self-Test Enable** -- Writing a logic "1" to this bit causes the module to disable power to all row and column drivers. This allows testing the operation of the FIFO, for example, without causing relay movement. Writing a logic "0" to this bit allows the row and column drivers to be powered (if driver power is enabled). Be sure that the FIFO is empty before returning this bit to logic "0".

**Driver Power Enable** -- Writing a logic "1" to this bit enables power to the relay drivers. Writing a logic "0" to this bit removes power from the relay drivers so that no relay movements are possible. When power is cycled, this bit resets to logic "0" to ensure that relays will not move unexpectedly. You must enable this bit before any relay movements can be done.

**Timer Mode Bit 2/1** -- These two bits set the amount of time the module will drive the relay coils. These values give some software control of the driving/settling times that may be useful for performance tuning as well as module testing.

**Note** Proper operation is guaranteed only for the 00 (8 msec) mode.

| TIMER MODE BIT 2 | TIMER MODE BIT 1 | Time   |
|------------------|------------------|--------|
| 0                | 0                | 8mSec  |
| 0                | 1                | 2mSec  |
| 1                | 0                | 4mSec  |
| 1                | 1                | 64mSec |

The following table shows the four possible settings.

Comments

• Changing the **Timer Mode**, **Self-Test**, or **Driver Power Enable** bits in the **Control Register** should only be done immediately after a reset or when the FIFO is empty and no relay operations are pending.

#### **Reserved Registers**

These registers are not available for use. You can write to them (but no data is stored) and reads always return all ones.

# Table 2-10. Reserved Registers (Read Only) Base + 04\_h through 0E\_h

| Bit Number | 15 - 00 |
|------------|---------|
| Bit Name   | Unused  |

**Reset Condition** -- Bits 15 - 00 = logic "1"

#### **Row Set and Reset Registers** The Switch M-Modules use a row and column relay drive scheme. To close a particular relay, write a logic "1" to the corresponding column in a **Row n Set** register. To open a relay, write a logic "0" in the corresponding column in a **Row n Reset** register. For example, to close the Channel 04 relay on the Racal M1701A (Row 1, Column 0 in relay drive scheme) place a logic "1" in bit 00 of the **Row 1 Set** register. To open this relay, place a logic "0" in bit 00 of the **Row 1 Reset** register. Tables 2-13 through 2-15 show the correlation of the matrix drive rows and columns to Switch M-Module channels.

**Reset Condition** (all **Row n Set** and **Row n Reset** registers) -- Bits 15 - 04 = logic "1", Bits 03 - 00 = logic "0". Bits 15 - 04 always read logic "1".

#### Table 2-11. Row 0 Set Register (Read/Write) Base + $10_{h}$

| Bit Number | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|------------|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name   | Unused  | Row 0<br>Column 3<br>State | Row 0<br>Column 2<br>State | Row 0<br>Column 1<br>State | Row 0<br>Column 0<br>State |

| Table 2-12. Row 0 Reset Register | r (Read/Write) Base + 12 <sub>h</sub> |
|----------------------------------|---------------------------------------|
|----------------------------------|---------------------------------------|

| Bit Number | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|------------|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name   | Unused  | Row 0<br>Column 3<br>State | Row 0<br>Column 2<br>State | Row 0<br>Column 1<br>State | Row 0<br>Column 0<br>State |

| Table 2-13. Row 1 Set Registe | r (Read/Write) Base + $14_h$ |
|-------------------------------|------------------------------|
|-------------------------------|------------------------------|

| Bit Number | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|------------|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name   | Unused  | Row 1<br>Column 3<br>State | Row 1<br>Column 2<br>State | Row 1<br>Column 1<br>State | Row 1<br>Column 0<br>State |

| Bit Number  | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|---|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name  | Unused  | Row 1<br>Column 3<br>State | Row 1<br>Column 2<br>State | Row 1<br>Column 1<br>State | Row 1<br>Column 0<br>State |
| Table 2-15. Row 2 Set Register (Read/Write) Base + 18 |         |                            |                            |                            |                            |
| Bit Number  | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
| Bit Name  | Unused  | Row 2<br>Column 3          | Row 2<br>Column 2          | Row 2<br>Column 1          | Row 2<br>Column 0          |

State

State

State

| Table 2-14. Row 1 Reset Register (Read/Write) Base + 16 |
|---|
|---|

Table 2-16. Row 2 Reset Register (Read/Write) Base +  $1A_h$ 

State

| Bit Number | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|------------|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name   | Unused  | Row 2<br>Column 3<br>State | Row 2<br>Column 2<br>State | Row 2<br>Column 1<br>State | Row 2<br>Column 0<br>State |

Table 2-17. Row 3 Set Register (Read/Write) Base + 1C<sub>h</sub>

| Bit Number | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|------------|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name   | Unused  | Row 3<br>Column 3<br>State | Row 3<br>Column 2<br>State | Row 3<br>Column 1<br>State | Row 3<br>Column 0<br>State |

| Table 2-18. Row 3 Reset Register | (Read/Write) Base + 1E <sub>h</sub> |
|----------------------------------|-------------------------------------|
|----------------------------------|-------------------------------------|

| Bit Number | 15 - 04 | 03                         | 02                         | 01                         | 00                         |
|------------|---------|----------------------------|----------------------------|----------------------------|----------------------------|
| Bit Name   | Unused  | Row 3<br>Column 3<br>State | Row 3<br>Column 2<br>State | Row 3<br>Column 1<br>State | Row 3<br>Column 0<br>State |

**Row n Column n State** -- When the FIFO is empty (no relay operations pending) bits 03, 02, 01, and 00 in the above registers indicate the state of the corresponding relay. A logic "1" means the relay in **Row n Column n** is closed or soon will be (depending on the **FIFO Empty Status** bit's state). A logic "0" means the corresponding relay is open.

Writing to a Row n Set register closes the relays only in the bit positions set to logic "1". Writing a logic "0" to a Row n Set register has no effect on relay position. Writing to a Row n Reset register opens relays only for the bit positions set to logic "0". Writing a logic "1" to a Row n Reset register has no effect on relay position.

- Reading either the **Row n Set** or **Row n Reset** register addresses returns identical data because they are actually mapped to the same register. When you write to one of these registers (and FIFO is not full), the data is stored in the register and stored in FIFO.
- The Row n Set/Reset readback registers return the programmed relay

state only if you use the module correctly. Since the driver power can be disabled (the power-on state), the **Row n Set** and **Row n Reset** registers can be written to and read from without moving any relay contacts.

- When the module loses power, any closed relays remain closed (latching relays). When power is restored, the relays remain closed but the **Row n Set** and **Row n Reset** registers have lost their relay state information. This relay information is lost whenever power is cycled or the carrier asserts /RESET. You must initialize the module after a power-up or /RESET to achieve correlation between the **Row n Set/Reset** readback registers and the actual relay positions. To initialize the module:
  - 1. Enable driver power.
  - 2. Write all four column bits to zero in each Row n Reset register.

You can check for initialization by reading the **Init Status** bit. If the module has not been initialized since the last power-up or /RESET, the **Init Status** bit will be logic "0". The **Init Status** bit is set to logic "1" whenever the module has been successfully initialized.

- To guarantee break-before-make relay operation, write to the **Row n Reset** registers before writing to the **Row n Set** registers.
- It is important to use the FIFO status bits when writing to the **Row n Set/Reset** registers, especially when writing in bursts (such as when resetting the module's relays). Writing to a **Row n Set/Reset** register when the FIFO is full results in the loss of data since the FIFO has no room to hold it. You should always check the FIFO FULL status to ensure that FIFO is not full before writing to a **Row n Set/Reset** register.

# Matrix Drive to Channel Mappings

Tables 2-13 and 2-15 correlate matrix drive rows and columns to channel numbers on the Racal M1701 and M1703, respectively. Table 2-14 correlates matrix drive rows and columns to Racal M1702 rows and columns.

| Matrix Drive | Column 0   | Column 1   | Column 2   | Column 3   |
|--------------|------------|------------|------------|------------|
| Row 0        | Channel 0  | Channel 1  | Channel 2  | Channel 3  |
| Row 1        | Channel 4  | Channel 5  | Channel 6  | Channel 7  |
| Row 2        | Channel 8  | Channel 9  | Channel 10 | Channel 11 |
| Row 3        | Channel 12 | Channel 13 | Channel 14 | Channel 15 |

| Matrix Drive | Column 0     | Column 1     | Column 2     | Column 3     |
|--------------|--------------|--------------|--------------|--------------|
| Row 0        | Row 0, Col 0 | Row 0, Col 1 | Row 0, Col 2 | Row 0, Col 3 |
| Row 1        | Row 1, Col 0 | Row 1, Col 1 | Row 1, Col 2 | Row 1, Col 3 |
| Row 2        | Row 2, Col 0 | Row 2, Col 1 | Row 2, Col 2 | Row 2, Col 3 |
| Row 3        | Row 3, Col 0 | Row 3, Col 1 | Row 3, Col 2 | Row 3, Col 3 |

Table 2-20. Racal M1702 Matrix Drive to Row and Column Mappings

|               | Matrix Drive | Column 0   | Column 1   | Column 2   | Column 3   |
|---------------|--------------|------------|------------|------------|------------|
|               | Row 0        | Channel 0  | Channel 1  | Channel 2  | Channel 3  |
| Multiplexer A | Row 1        | Channel 4  | Channel 5  | Channel 6  | Channel 7  |
|               | Row 2        | Channel 8  | Channel 9  | Channel 10 | Channel 11 |
| Multiplexer B | Row 3        | Channel 12 | Channel 13 | Channel 14 | Channel 15 |

# **Unused Registers**

These registers can be written to (but no data is stored) and read from (but always returns all ones).

| Table 2-22. Unused Registers (Read Only) | Base + $20_{h}$ through $7E_{h}$ |
|--|----------------------------------|
|--|----------------------------------|

| Bit Number | 15     | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|------------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bit Name   | Unused |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Reset Condition** -- Bits 15 - 00 = logic "1"

ID EEPROM<br/>RegisterThe ID EEPROM Register allows you to access the contents of the ID<br/>EEPROM. The ID EEPROM contains sixty-four 16-bit words of M-Module<br/>ID data and VXI M-Module data.

**Note** It is much easier to read the module ID data from the VXI registers (A16 memory area) instead of reading the ID EEPROM Register. A16 addressing is discussed earlier in this chapter

| Bit Number | 15 - 03 | 02             | 01    | 00             |
|------------|---------|----------------|-------|----------------|
| Bit Name   | Unused  | Chip<br>Select | Clock | Data<br>In/Out |

**Reset Condition** -- Bits 15 - 08 = logic "1", Bits 07 - Bit 00 = logic "0". Reads of bit-0 reflect the state of the ID EEPROM's DO pin.

# Caution Do not attempt to write to Bit 00 of the ID EEPROM register. You could possibly write-over the contents of the ID EEPROM.

**Bit Definitions** Data In/Out -- Reading this bit returns the value returned from the Data Out pin of the ID EEPROM.

**Clock** -- Writing a logic "1" to this bit forces the SK pin of the ID EEPROM high and writing a logic "0" drives it low. This bit is used as a clock to the ID EEPROM for reading data out. Reading this bit always returns a logic "0".

**Chip Select** -- Writing a logic "1" to this bit selects the ID EEPROM. Writing a logic "0" to this bit deselects the EEPROM. Reading this bit always returns a logic "0".

| Word Number | Description                      | Racal M1701 Form A<br>Switch             | Racal M1702 4x4<br>Matrix                | Racal M1703<br>Multiplexer               |
|-------------|----------------------------------|--|--|--|
| 0           | Sync Code                        | 5346 <sub>h</sub>                        | 5346 <sub>h</sub>                        | 5346 <sub>h</sub>                        |
| 1           | M-Module Number<br>(binary code) | 0686 <sub>h</sub><br>(binary-coded 1670) | 0687 <sub>h</sub><br>(binary-coded 1671) | 0688 <sub>h</sub><br>(binary-coded 1672) |
| 2           | Revision Number<br>(binary code) | 0001 <sub>h</sub>                        | 0001 <sub>h</sub>                        | 0001 <sub>h</sub>                        |
| 3           | Module<br>Characteristics        | 0860 <sub>h</sub>                        | 0860 <sub>h</sub>                        | 0860 <sub>h</sub>                        |
| 4 - 15      | Reserved                         | n/a                                      | n/a                                      | n/a                                      |
| 16          | VXI Sync Code                    | ACBA <sub>h</sub>                        | ACBA <sub>h</sub>                        | ACBA <sub>h</sub>                        |
| 17          | VXI ID                           | $CFFF_h$                                 | CFFF <sub>h</sub>                        | CFFF <sub>h</sub>                        |
| 18          | VXI Device Type                  | F25B <sub>h</sub>                        | F25C <sub>h</sub>                        | F25D <sub>h</sub>                        |
| 19 - 63     | Reserved                         | n/a                                      | n/a                                      | n/a                                      |

#### Table 2-24. ID EEPROM Contents

# **M-Module Specification Compliance**

The Switch M-Modules comply with the Mezzanine M-Module Specification.

# **Racal M1701 16-Channel Form A Switch Specifications**

Caution The following voltage limits designated "Cleanroom Environment" apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and NO relay connection is made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

# Maximum Voltage--Cleanroom Environment (any terminal to any other terminal)

- 200 VDC
- 125 VAC rms
- 175 VAC peak

# Maximum Voltage--Non-Cleanroom Environment (any terminal to any other terminal)

- 60 VDC
- 48 VAC rms
- 68 VAC peak

#### Maximum Current (non-inductive)

- Per Switch: 2 ADC, 2 AAC peak
- Per Module: 8 ADC, 8 AAC peak

#### **Maximum Power**

- Per Switch: 50 W DC, 50 VA AC
- Per Module: 200 W DC, 200 VA AC

#### **Racal M1701 Specifications (continued)**

#### Maximum Thermal Offset

• < 3  $\mu$ V (typical)

#### **Closed Channel Resistance**

- Initial:  $< 0.2\Omega$  (typical)
- End of Life:  $< 2\Omega$

#### Insulation Resistance (between any two points)

- $\leq 40^{\circ}$ C,  $\leq 65\%$  RH:  $10^{8} \Omega$  (typical)
- $\leq 25^{\circ}$ C,  $\leq 40\%$  RH:  $10^{8} \Omega$  (typical)

#### **AC Specifications**

- Typical Bandwidth (-3dB): > 10 MHz
- Crosstalk (dB, channel-to-channel):
  - <100 kHz: -64 dB (typical)
  - <1 MHz: -44 dB (typical)
  - <10 MHz: -24 dB (typical)
- Closed Channel Capacitance: Channel-to-Channel: < 15 pF (typical) Channel-to-Common: < 25 pF (typical)

#### **General Characteristics**

- 16 Latching Relays
- Typical Relay Life (number of operations):
  - Rated Load: 10<sup>5</sup>

Time to open or close a channel (register programming): 8 msec

- Connector Type: 44-pin D-Sub
- Standard Compliance: IDENT, A08, D08, INTC
- Field Wiring Connector: 44-pin D-Sub (male) with plastic housing
- VXI Device Type: Register-Based
- Interrupt: Type C interrupt when requested relay movements have completed.

#### **Power Up/Down States**

Latching relays retain last programmed state.

# **Racal M1702 4x4 Matrix Switch Specifications**

Caution The following voltage limits designated "Cleanroom Environment" apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and NO relay connection is made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

Maximum Voltage--Cleanroom Environment (any terminal to any other terminal)

- 200 VDC
- 125 VAC rms
- 175 VAC peak

# Maximum Voltage--Non-Cleanroom Environment (any terminal to any other terminal)

- 60 VDC
- 48 VAC rms
- 68 VAC peak

#### Maximum Current (non-inductive)

- Per Channel: 2 ADC, 2 AAC peak
- Per Module: 8 ADC, 8 AAC peak

#### **Maximum Power**

- Per Channel: 50 W DC, 50 VA AC
- Per Module: 200 W DC, 200 VA AC

#### Maximum Thermal Offset Per Channel, Differential Hi-Lo

• < 3  $\mu$ V (typical)

#### **Closed Channel Resistance**

- Initial:  $< 0.3\Omega$  (Hi or Lo) (typical)
- End of Life:  $< 2\Omega$  (Hi or Lo)

#### Insulation Resistance (between any two points)

- $\leq 40^{\circ}$ C,  $\leq 65\%$  RH:  $10^{8} \Omega$  (typical)
- $\leq 25^{\circ}$ C,  $\leq 40\%$  RH:  $10^{8} \Omega$  (typical)

#### **Racal M1702 Specifications (continued)**

#### **AC Specifications**

- Typical Bandwidth (-3dB): > 10 MHz
- Crosstalk (dB, channel-to-channel):
  - <100 kHz: -64 dB (typical)
  - <1 MHz: -44 dB (typical)
  - <10 MHz: -24 dB (typical)
- Closed Channel Capacitance: Hi-Lo: < 40 pF (typical) Hi-Chassis: < 60 pF (typical) Lo-Chassis: < 60 pF (typical)</li>

#### **General Characteristics**

- 16 Latching Relays
- Typical Relay Life (number of operations)
  - Rated Load: 10<sup>5</sup> (typical)

Time to open or close a channel (register programming): 8 msec

- Connector Type: 44-pin D-Sub
- Standard Compliance: IDENT, A08, D08, INTC
- Field Wiring Connector: 44-pin D-Sub (male) with plastic housing
- VXI Device Type: Register-Based
- Interrupt: Type C interrupt when requested relay movements have completed.

#### **Power Up/Down States**

Latching relays retain last programmed state.

# **Racal M1703 Dual 8-to-1 Relay Multiplexer Specifications**

Caution The following voltage limits designated "Cleanroom Environment" apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and NO relay connection is made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

Maximum Voltage--Cleanroom Environment (any terminal to any other terminal)

- 200 VDC
- 125 VAC rms
- 175 VAC peak

# Maximum Voltage--Non-Cleanroom Environment (any terminal to any other terminal)

- 60 VDC
- 48 VAC rms
- 68 VAC peak

#### Maximum Current (non-inductive)

- Per Channel: 2 ADC, 2 AAC peak
- Per Module: 8 ADC, 8 AAC peak

#### **Maximum Power**

- Per Channel: 50 W DC, 50 VA AC
- Per Module: 50 W DC (16-to-1 mode), 100 W DC (8-to-1 mode) 50 VA AC (16-to-1 mode), 100 VA AC (8-to-1 mode)

#### Maximum Thermal Offset Per Channel, Differential Hi-Lo

• < 3  $\mu$ V (typical)

#### **Closed Channel Resistance (per channel)**

- Initial:  $< 0.2\Omega$  (typical)
- End of Life:  $< 2\Omega$

#### Insulation Resistance (between any two points)

- $\leq 40^{\circ}$ C,  $\leq 65\%$  RH:  $10^{8} \Omega$  (typical)
- $\leq 25^{\circ}$ C,  $\leq 40\%$  RH:  $10^{8} \Omega$  (typical)

#### **Racal M1703 Specifications (continued)**

#### **AC Specifications**

- Typical Bandwidth (-3dB): > 10 MHz
- Crosstalk (dB, channel-to-channel):
  - <100 kHz: -64 dB (typical)
  - <1 MHz: -44 dB (typical)
  - <10 MHz: -24 dB (typical)
- Closed Channel Capacitance:

Ch-Ch: < 20 pF (8-to-1 mode), < 25 pF (16-to-1 mode) (typical) Hi-Lo: < 40 pF (8-to-1 mode), < 70 pF (16-to-1 mode) (typical) Ch-Ch: < 75 pF (8-to-1 mode), < 140 pF (16-to-1 mode) (typical)

#### **General Characteristics**

- 16 Latching Relays
- Typical Relay Life (number of operations)
  - Rated Load: 10<sup>5</sup> (typical)

Time to open or close a channel (register programming): 8 msec

- Connector Type: 44-pin D-Sub
- Standard Compliance: IDENT, A08, D08, INTC
- Field Wiring Connector: 44-pin D-Sub (male) with plastic housing
- VXI Device Type: Register-Based
- Interrupt: Type C interrupt when requested relay movements have completed.

#### **Power Up/Down States**

Latching relays retain last programmed state.

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#### **Racal Instruments**

#### **REPAIR AND CALIBRATION REQUEST FORM**

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Repair Facility.

| ModelSer   | ial No [  | Date            |  |  |  |  |  |  |
|--|---|-----------------|--|--|--|--|--|--|
| Company Name   | Purchase Orde   | er #            |  |  |  |  |  |  |
| Billing Address  |   |                 |  |  |  |  |  |  |
|  | City  |                 |  |  |  |  |  |  |
| State/Province   | Zip/Postal Code   | Country         |  |  |  |  |  |  |
| Shipping Address   |   |                 |  |  |  |  |  |  |
|  | City  |                 |  |  |  |  |  |  |
| State/Province   | Zip/Postal Code   | Country         |  |  |  |  |  |  |
| Technical Contact  | Phone Number ( )  |                 |  |  |  |  |  |  |
| Purchasing Contact   |   |                 |  |  |  |  |  |  |
| details, such as input/output lev<br>2. If problem is occurring when   | em and symptoms you are havi<br>vels, frequencies, waveform det<br>unit is in remote, please list the | tails, etc.     |  |  |  |  |  |  |
| controller type.   |   |                 |  |  |  |  |  |  |
|  | formation you feel would be be<br>etc.)   |                 |  |  |  |  |  |  |
|  |   |                 |  |  |  |  |  |  |
|  |   |                 |  |  |  |  |  |  |
| 4. Is calibration data required?                                       | Yes No (please circle   | one)            |  |  |  |  |  |  |
| Call before shipping<br>Note: We do not accept<br>"collect" shipments. | Ship instruments to nearest   | support office. |  |  |  |  |  |  |